**EL 426**

**Practice Problem Session**

**Q – 1**

Consider the following pseudo-assembly code:

R6=500

R7=0

R9=0

**SOURCE:** R12=MEM[R6+0] **// Load from the memory**

if(R12>0) goto **DEST** **// Branch 1** – **Notice the target!**

R7=R7+1, R9=R9+R12

R9=R9+R7

R9=R9/2

**INTER:** if(R12>=0) goto **DEST** **// Branch 2**

R9=R9+1

**DEST:** R6=R6+4

if(R7<50000) goto **SOURCE** **// Branch 3**

“SOURCE” has an address of 0x100. The predictors all use the least significant bits of the PC other than the word-offset. Predictors and patterns are all initialized to all zeros (not taken).

You are to consider how different branch predictors will behave on this code under different circumstances.

**Case 1:** The data loaded from memory is 1 the first time, 0 the second, 1 the third, 0 the forth and follows that pattern forever (1, 0, 1, 0, 1, 0, etc.)

**Case 2:** The data loaded from memory is 0 the first time, -1 the second, -1 the t hird, -1 the forth and follows that pattern forever (0, -1 -1, -1, 0, -1, -1, -1, etc.)

**Case 3:** The data loaded is (1, 0, -1, 1, 0, -1, 1, 0, -1, etc.)

You are now to consider 2 branch predictors:

**Predictor 1:** A PC-based predictor with 8 entries each a 1 bit predictor.

**Predictor 2:** A local pattern history predictor. The BHT has 16 entries, each with 2 bits of history. The predictors are each 1 bit.

What are the expected prediction *rates* for each of the following (percentage of time right)? Your answers must be correct within 1.0%.

Provide your final answer in the following table format

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Case 1 | | Case 2 | | Case 3 | |
| Predictor 1 | Predictor 2 | Predictor 1 | Predictor 2 | Predictor 1 | Predictor 2 |
| Branch 1 | 50 | 100 | 0 | 75 | 33 | 66 |
| Branch 2 | 100 | 100 | 50 | 75 | 0 | 50 |
| Branch 3 | 50 | 100 | 0 | 100 | 33 | 100 |